

## Patent Assignment Abstract of Title

**Total Assignments: 1**

**Application #:** 09751719 **Filing Dt:** 12/29/2000

**Patent #:** NONE

**Issue Dt:**

**PCT #:** NONE

**Publication #:** NONE

**Pub Dt:**

**Inventors:** Dennis M. Briddell, Chirag Shroff

**Title:** Switching fabric for interfacing a host processor and a plurality of network modules

**Assignment: 1**

**Reel/Frame:** 011569/0291

**Received:**  
03/13/2001

**Recorded:**  
03/01/2001

**Mailed:**  
05/15/2001

**Pages:**  
5

**Conveyance:** ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

**Assignors:** BRIDDELL, DENNIS M.

**Exec Dt:** 01/04/2001

SHROFF, CHIRAG

**Exec Dt:** 12/23/2000

**Assignee:** CISCO TECHNOLOGY, INC.

170 WEST TASMAN DRIVE  
SAN JOSE, CALIFORNIA 95134

**Correspondent:** BAKER BOTTS L.L.P.

BARTON E. SHOWALTER  
2001 ROSS AVENUE  
DALLAS, TX 75201-2980

Search Results as of: 5/20/2004 4:50:30 P.M.

---

If you have any comments or questions concerning the data displayed, contact OPR / Assignments at 703-308-9723  
Web Interface last modified: Oct. 5, 2002

## Refine Search

### Search Results -

Term	Documents
LAYER	818897
LAYERS	483116
(28 AND LAYER).USPT.	2
(L28 AND LAYER ).USPT.	2

Database:

US Pre-Grant Publication Full-Text Database  
 US Patents Full-Text Database  
 US OCR Full-Text Database  
 EPO Abstracts Database  
 JPO Abstracts Database  
 Derwent World Patents Index  
 IBM Technical Disclosure Bulletins

Search:

L29





### Search History

 DATE: Thursday, May 20, 2004    [Printable Copy](#)    [Create Case](#)

#### Set Name Query

side by side

DB=USPT; PLUR=YES; OP=ADJ

L29    L28 and layer  
 L28    L27 and ATM  
 L27    L25 and protocol  
 L26    L25 and peer  
 L25    L24 and modules  
 L24    L23 and interface  
 L23    L22 and bus adj controller  
 L22    switch adj fabric and PCI  
 L21    L20 and host  
 L20    L19 and bus adj controller  
 L19    L18 and fabric

#### Hit Count Set Name

result set

2    L29  
 2    L28  
 5    L27  
 2    L26  
 6    L25  
 6    L24  
 6    L23  
 157    L22  
 1    L21  
 1    L20  
 4    L19

<u>L18</u>	peer adj controller	16	<u>L18</u>
<u>L17</u>	peer adj transaction adj controller	0	<u>L17</u>
<u>L16</u>	L15 and PCI	1	<u>L16</u>
<u>L15</u>	L14 and processor	4	<u>L15</u>
<u>L14</u>	L13 and interface	4	<u>L14</u>
<u>L13</u>	L12 and modules	4	<u>L13</u>
<u>L12</u>	L11 and fabric	7	<u>L12</u>
<u>L11</u>	370/421.ccls.	75	<u>L11</u>
<u>L10</u>	peer adj transaction adj bus	0	<u>L10</u>
<u>L9</u>	17 and fabric	0	<u>L9</u>
<u>L8</u>	L7 and switch adj fabric	0	<u>L8</u>
<u>L7</u>	L6 and peer	2	<u>L7</u>
<u>L6</u>	plurality adj modules and interface and transaction adj bus	24	<u>L6</u>
<u>L5</u>	L3 and bus	2	<u>L5</u>
<u>L4</u>	L3 and transaction adj bus	0	<u>L4</u>
<u>L3</u>	L1 and processor and interface	2	<u>L3</u>
<u>L2</u>	L1 and processor adj interface	0	<u>L2</u>
<u>L1</u>	switch adj fabric and plurality adj module adj interfaces	2	<u>L1</u>

END OF SEARCH HISTORY